

## Silicon Interposers with Integrated Passive Devices: Ultra-Miniaturized Solution using 2.5D Packaging Platform

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### Abstract

This paper addresses one of the most promising technologies that meets the demand in terms of miniaturization and increased performance. IPDiA has developed a range of silicon interposers which, when combined with Integrated Passive Devices (IPD) and Through Silicon Vias (TSV), offer a new solution to related portable products, implantable medical devices, avionics and defense.

### Keywords

*2D Silicon Interposers, 2.5D Silicon Interposers, Through Silicon Via, Integration, Miniaturization, 3D Packaging, Integrated Passive Devices.*

### Introduction

The common point with articles relating progress in the electronic components world is the search for form factor reduction and high performance. Since the 90s, designers have been working on 3D integration (Multi-Chip Package, stacked die, System in Package) which brings highly efficient solutions to achieve these goals. Several products have been developed, in particular the interposers. The interposer can be assimilated to a packaging platform serving as a high density substrate with a redistribution layer and offering, unlike traditional packages, the reduced pitch capabilities required by advanced IC technology nodes [1]. In other words, the interposer plays the role of a space transformer from the IC to the applicative module. It also allows usually incompatible technologies to be mixed on the same platform, therefore leading to heterogeneous integration (System in Package on interposer) [2]. Combined with Through Silicon Vias, it opens the doors to an optimized form factor world (system volume, weight and footprint) with improved performance (higher transmission speed, lower power consumption and RF parasitic reduction).

From an applicative point of view, interposers were first imagined to be used as a pure packaging platform dedicated to dies with large I/O number (high density BGA). They have evolved towards 3D structures to meet the demands of CCD imager, mobile phone and consumer applications. Now, an additional range of applications can be reached with the so-called 2.5D interposers. This new approach offers an economic model perfectly adapted to related portable products, implantable medical devices, avionics and defense.

Several types of material can be considered as interposer substrate, each offering intrinsic properties that need to be seriously considered prior to any other considerations. Silicon is one, and is chosen for the following reasons: first, silicon is a stable base substrate that presents a very small CTE (coefficient of thermal expansion) mismatch with attached external ICs. Since the active parts are in fact often made of silicon themselves, the thermo-mechanical stresses encountered during processing and lifetime application are minimized, thereby increasing the reliability. Silicon therefore offers a very good trade-off between thermal conductivity and thickness. It is also perfectly adapted to via or micro-via technology (including via last technology) and provides wider possibilities in terms of pitch, via diameter and via density. Lastly, it enables passive devices to be integrated (IPD technology) and is compatible with ICs and MEMS.

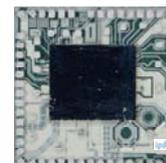
The interposers can be divided into three families. The three structures show the common key advantages of enabling external integration of active dies without their packaging, as well as integration (externally or internally) of passive devices.

#### - 2D Silicon Interposer:

This two vertical stage structure is an intermediate solution in terms of footprint. Due to the connections from the sides of the interposer to the final module, space saving is not totally optimized. However, combined with a wide range of integrated passive devices (high-density trench capacitors, MIM capacitors, resistors, high-Q inductors) and external active dies [3], this may represent a very good compromise for cost-driven applications such as in the mobile market.

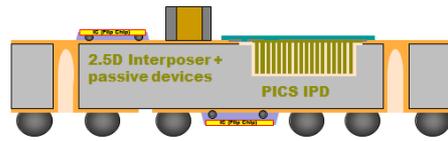


**Fig. 1a:** Schematic of IPDiA 2D interposer with PICS IPD and external active dies in flip-chip or chip-on-silicon technologies



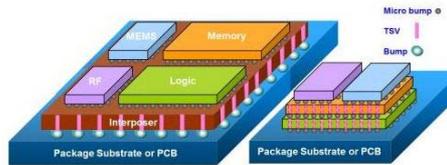
**Fig. 1b:** IPD RF module for W-CDMA & GSM RF transceiver

- **2.5D Silicon Interposer:**  
This is also a two vertical stage structure. The difference comes from the copper vias which, combined with IPDs, provide a higher level of integration together with system performance improvements. This structure also allows external component integration on the top and on bottom.



**Fig. 2:** Schematic of IPDiA 2.5D interposer with PICS IPD and external active dies in flip-chip or chip-on-silicon technologies

- **3D interposer:**  
In this case, the structure is a multistage integration and all layers are active. Although the 3D structure could be interesting in terms of miniaturization, it still shows too many drawbacks in terms of design flow, testing, cost, stress impact and thermal issues [4] and will not be addressed in this article.



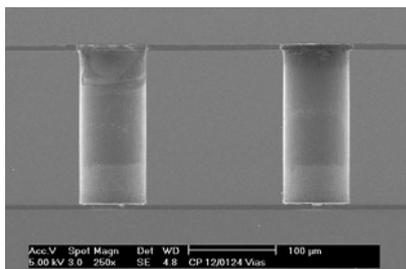
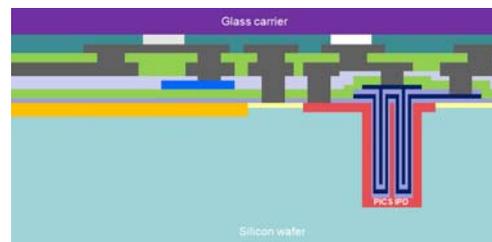
**Fig. 3:** Comparison between 2.5D and 3D interposer structures [5]

Now that some general points about interposers have been described, we will explore what has been developed so far to optimize the performance and density of these devices. For a better understanding of the results presented, the TSV process flow set up by IPDiA R&D experts will first be detailed. Some design rules will then be given, followed by comparison tables and characterizations. The reliability model tested will also be described. Finally, some applicative examples involving interposers will be detailed. The IPD process will not be developed here, however numerous articles are available on the subject [6], [7].

**TSV key process steps**

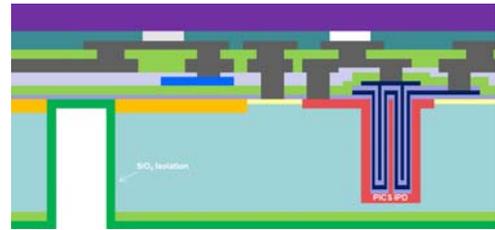
The introduction of Through Silicon Vias has a tremendous positive impact on new 3D packaging architectures. TSVs enable higher density and shorter connection lengths compared with wire bonded solutions and are perfectly fitted to face the increasing demand for faster signals and lower power use. IPDiA is providing TSVs for interposers with or without IPDs. In the past years, IPDiA and its main technological partner CEA-Leti have worked on TSV process optimization to bring it to the right level of maturity and cost for markets where high added-value products are needed (medical devices, aerospace, professional electronics and telecom infrastructures). Of the three TSV process options (via first, via middle and via last), IPDiA endorsed the via last approach, in which vias are formed after the die has been manufactured. This choice is mainly driven by co-integrating TSV with IPDiA PICS technology (Passive Integration Connecting Substrate). Moreover, this solution brings the potential of making TSV on pre-existing CMOS wafer or on a 2.5D IPD interposer developed by IPDiA [8]. The TSV key process steps are listed below:

- **Bonding process:** temporary wafer bonding carried out on a glass substrate is necessary to make thin wafer handling possible through the next steps at process temperatures up to 250 °C.



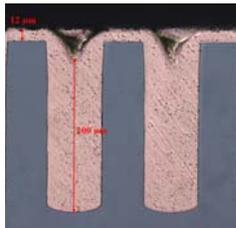
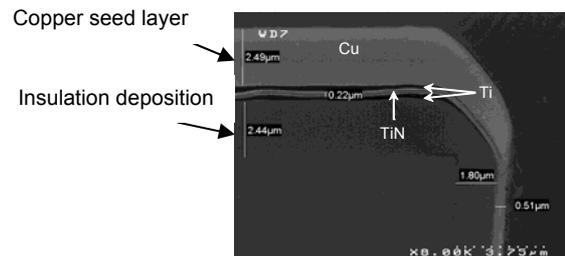
- **Deep silicon etching:** due to the bonding process, silicon etching is made from the back side to the first dielectric on the front side. During this step, the undesirable notching effect at the bottom of the via is minimized and the thickness variations are absorbed, preparing the ground for functional and efficient vias.

- **Insulation deposition:** an SiO<sub>2</sub> layer is deposited to provide the insulation needed between the lateral parts of the vias and the substrate. At this stage, a thickness ratio of 0.25 between the bottom corner and the top plan and a relative permittivity of 5 are measured, which leads us to conclude that conditions are right for the propagation of RF signals through the TSV with limited attenuation.



- **Etch back:** the insulation film and the first silicon dielectric are removed from the bottom of the cavities with an etching step using a gas mixture consisting mainly of Ar for an efficient vertical etch. Cooling steps are necessary to preserve the wafer bonding glue.

- **Barrier and seed deposition:** the efficiency of the copper filling depends on the characteristics of underlying barrier and seed layers. Ti is used as an adherence layer and TiN as a barrier against Cu diffusion into the interposer silicon structure.



- **Copper via filling and back side metallization:** at this stage, both copper via filling and back side metallization (tracks) are carried out. In order to modulate the copper thickness at the bottom of vias while limiting the thickness at the surface, IPDiA developed 'super-filling' obtained with electrochemical deposition and pulsed current. The 'super-filling' enables to facilitate the final module assembly.

- **Passivation and finishing:** after the seed layer etching, a final passivation step using organic material is performed to complete the wafer back-side and clog the via holes to prevent corrosion. Finishing prepares the assembly step with micro-bumps made at the back side of the interposer.

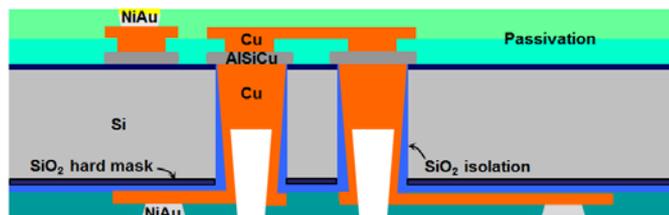
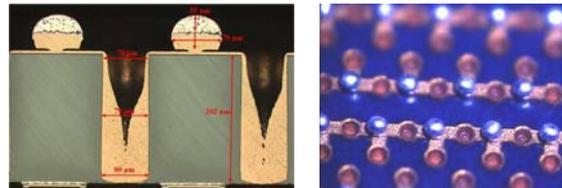


Fig. 4: Schematic view of the via final architecture

### Main design rules

In order to guide the architect in the integration of all external components within the interposer platform and to optimize a high level of integration, specific design rules on TSV interposer component have been defined by IPDiA and summarized in the table below:

PARAMETERS	SPECIFICATIONS
Interposer Thickness (Without Via)	[100 $\mu\text{m}$ ; 400 $\mu\text{m}$ ]
Interposer Thickness (With Via)	300 $\mu\text{m}$ standard
TSV diameter	75 $\mu\text{m}$ (Copper)
Vias filling	Copper or Non metal
Barrier layer	Optional
Finition 0	Optional
Finition 1	Optional
Via minimum pitch	125 $\mu\text{m}$
Layer 0 metal thickness	Copper 4 to 8 $\mu\text{m}$ upon request
Layer 1 metal thickness	Aluminum 1 $\mu\text{m}$
Layer 2 metal thickness	Copper 10 to 15 $\mu\text{m}$
Layer 0 metal minimum width	8 $\mu\text{m}$
Layer 1 metal minimum width	1.5 $\mu\text{m}$
Layer 2 metal minimum width	8 $\mu\text{m}$
Minimum space between 2 metal lines (Layer 0)	8 $\mu\text{m}$
Minimum space between 2 metal lines (Layer 1)	4 $\mu\text{m}$
Minimum space between 2 metal lines (Layer 2)	6 $\mu\text{m}$

**Table 1:** Main design rules for interposer with IPDs and vias

### Dimensional comparison table

Main dimensional characteristics for different types of substrate are summarized in the table below.

Substrate	Printed Circuit Board (PCB)	Thick/thin flex	Ceramic	Silicon Interposer
Line width / Spacing	90 $\mu\text{m}$ down to 65 $\mu\text{m}$ for advanced PCB technologies	75 $\mu\text{m}$ down to 50 $\mu\text{m}$ for advanced thin flex technologies	75 $\mu\text{m}$ to 50 $\mu\text{m}$ for advanced LTCC technologies	5 $\mu\text{m}$
	Accuracy around 25 $\mu\text{m}$	Accuracy around 15 $\mu\text{m}$	Accuracy around 15 $\mu\text{m}$ or less for LTCC	Less than 1 $\mu\text{m}$
Metal layers for signal & routing management	One metal layer in between 2 thick laminated layers	Two layers for advanced flex technology	One layer	No limitation (2 to 3 layers)
Via diameter	200 $\mu\text{m}$ or less for advanced PCB	150 $\mu\text{m}$ for the best in class	120 $\mu\text{m}$ for advanced LTCC	75 $\mu\text{m}$ or less

**Table 2:** Comparison with several substrates of dimensional features

### Thermal and thermo-mechanical comparison table

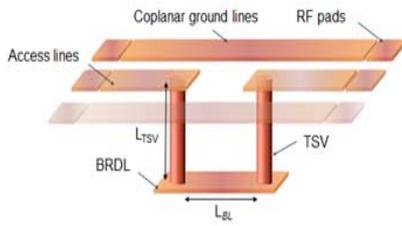
Main thermal and thermo-mechanical characteristics for different types of substrate are summarized in the table below.

Substrate	Printed Circuit Board (PCB)	Thick flex	Ceramic	Silicon Interposer
CTE1	~ 20 ppm/K	~ 20 ppm/K	~ 10 ppm/K	~ 2 ppm/K
	Big CTE mismatch with Silicon based ASIC	Big CTE mismatch with Silicon based ASIC	Slight CTE mismatch with Silicon based ASIC	No CTE mismatch with Silicon based ASIC
Temperature	Limited to 250 °C with warpage	Lower than 200 °C with polymer degradation	Higher than 400 °C for HTCC. Lower than 300 °C for LTCC	Higher than 300 °C
Packaging Process Compatibility	Very good with SMD	Good with SMD	Good with SMD	Good with SMD
	Specific adjustment with silicon die set	Good with silicon die set	Specific adjustment with silicon die set	Very good with silicon die set

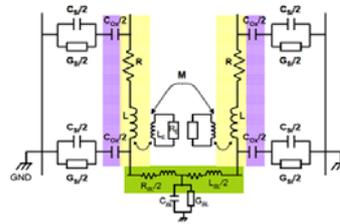
**Table 3:** Comparison with several substrates of thermal and thermo-mechanical features

**Electrical characterization**

All the results presented in the Electrical Characterization and the Reliability Model paragraphs refer to [8]. Based on the process described above, wafers have been processed and characterized in HF mode from which a  $\pi$ -shape equivalent model is validated. The results of the TSV performance are measured at High Frequency (HF) on a specific test structure called a Dual Via Chain (DVC) including CPW (Co-Planar Waveguide) adapted access, 2 TSV and a back side layer, as shown below.

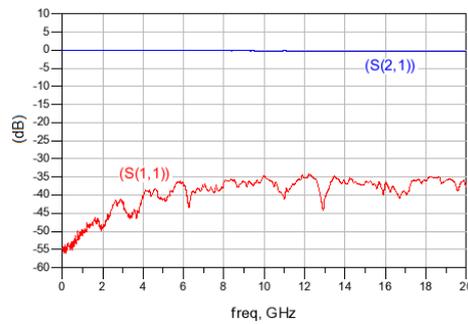


**Fig. 5a:** Dual Via Chain schematic view



**Fig. 5b:** Equivalent electrical schematic

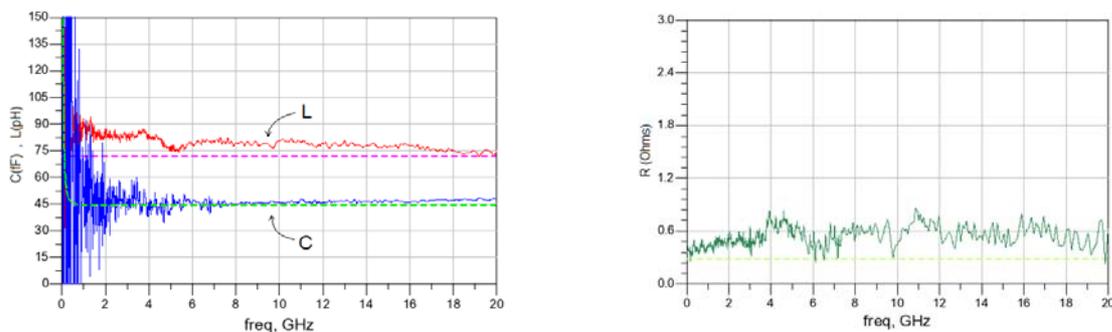
HF results are presented on figure 6. It represents the transmission and reflection of a 250  $\mu\text{m}$  length DVC.



**Fig. 6:** HR measurement result.  
Transmission (S21 in blue) and reflection (S11 in red)

The excellent result of this DVC shows a rejection between transmission and reflection of more than 35 dB throughout the frequency range (up to 20 GHz), and a very low loss in transmission, better than 0.35 dB. This performance is obtained thanks to control of the process, particularly with efficient contact between the copper in vias and the first metal layer on the front side, and the insulation of the TSV even on its critical corner in the bottom.

As shown on figure 7 below, we can conclude that the use of HR silicon has consistently reduced conductive loss in DVC of TSV. The high value of resistance introduced by the use of HR substrate makes it less sensitive to noise effect.



**Fig. 7:** Simulation (dashed line) and measurement (solid line) of extracted TSV  $\pi$ -shape elements.  
Parallel capacitance and series inductance (left), series resistance (right).

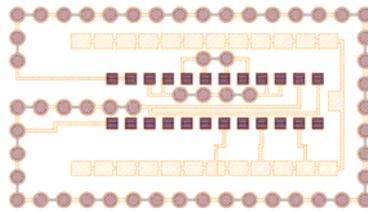
The table below summarizes some of the electrical performance and behavior of IPDiA TSV technology.

Designation	Value	Comments
Die thickness	200 $\mu\text{m}$ typ	
Via diameter	75 $\mu\text{m}$	
Via pitch	125 $\mu\text{m}$	
Via density	Max 64 Vias/ $\text{mm}^2$	
Via filling	Copper	
Insulation breakdown voltage	>200 V	
Serial resistivity per via	< 10 m $\Omega$	See curve for details < 10 m $\Omega$ up to 5 GHz
Serial inductor per via	< 100 pH	See curve for details ~50 pH up to 10 GHz
Via to via capacitance	< 1 pF	
IPD Generation	PICS2C	Passive components such as high density trench capacitors (80 nF/ $\text{mm}^2$ ), MIM capacitors (80 pF/ $\text{mm}^2$ ), resistors and high-Q Cu inductors

**Reliability model**

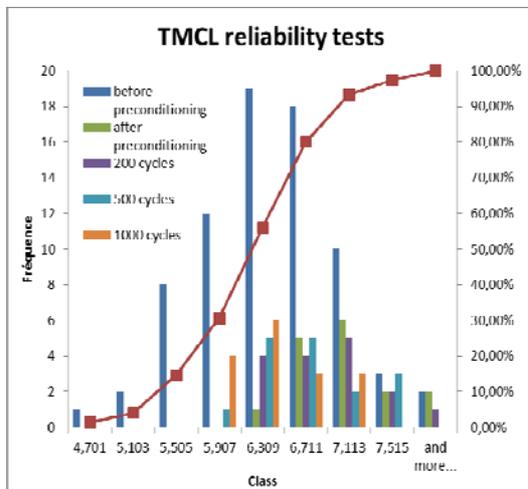
In order to test the ability to withstand cyclical exposure and introduce mechanical stress into TSV, they were subjected to thermal cycling (TMCL) as recommended by JEDEC standard [9] (cycling: -40 °C to 125 °C with a 10 °C/min ramp, during 200, 500 and 1000 cycles)

Figure 8 shows the layout of the structure used for this study. The DC resistance of a daisy chain made of 50 TSV is measured by a 4 point probe system.



**Fig. 8:** Daisy chain (50 TSV) used for the reliability tests.

Figure 9 shows the electrical results after this thermo-mechanical stress. Preconditioning was made on a full wafer (74 DVC structures) and TMCL reliability tests on ¼ wafer (16 DVC structures).



Statistics	Before Precond.	0 cycles	200 cycles	500 cycles	1000 cycles
Average	6,193	6,886	6,721	6,516	6,240
error deviation	0,073	0,126	0,119	0,110	0,101
median	6,172	6,869	6,714	6,520	6,236
standard deviation	0,630	0,487	0,459	0,440	0,404
sample variance	0,396	0,237	0,211	0,194	0,163
number of samples	74	16	16	16	16
Confidence interval (95.0%)	0,146	0,270	0,254	0,235	0,215

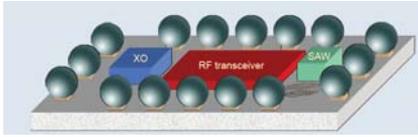
**Fig. 9:** Statistic chart and table on DC resistance results after TMCL reliability test

The Normal distribution of DC resistance on full wafer test (blue bar chart) and the cumulative distribution function (red curve) validates a good uniformity on full wafer for TSV chain structure. Note that the TMCL reliability test has been done on a ¼ wafer having the structure with the higher resistance. Moreover the low number of structure induces a non-Normal distribution. However, the low confidence interval on them reveals good uniformity and therefore good process maturity. The small and successive decreases in DC resistance can be interpreted as a crystalline rearrangement of copper introduced by successive cycling. This statistical approach allows us to estimate single TSV resistance to 124 m $\Omega$  with a very high accuracy, i.e. error less than 2%.

**Application examples**

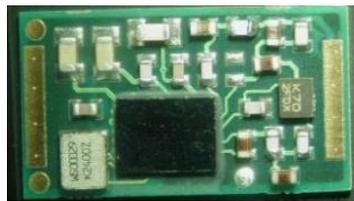
The application examples given below come as a conclusion of this article and illustrate perfectly the benefits of the different types of interposer in three specific areas (implantable medical devices, vision care devices and aerospace).

1/ 2D silicon interposer with IPD for implantable medical devices

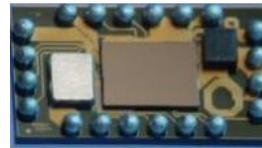


**Fig. 10:** RF module for medical application using IPDiA 2D interposer technology [10] [11]

In this first example, major improvements have been brought by IPDiA 2D interposer with Integrated Passive Devices to a medical sensor module including RF communication. The module is to be used in an implantable defibrillation system. The main concerns of the customer are miniaturization (size and weight impacts), stability and reliability. As described in the introduction of this article, the silicon not only serves as a redistribution layer but also allows the integration of passive components within the substrate. It enables a great size reduction (35% area saving, figure 11) and a decrease of the total system weight.



116 mm<sup>2</sup> / 1.6 mm height



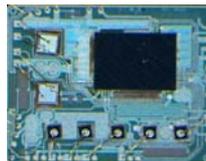
72 mm<sup>2</sup> / 1.2 mm height

**Fig. 11:** Comparison of module area between standard SMD technology (left) and IPDiA technology PICS (right)

Additionally, the PICS technology used for integration of the passive components results in very stable high capacitor integration. Finally, IPDiA offers a complete service with its stable flip-chip technology and the silicon-silicon compatibility between the substrate and the active dies meets the customer's demand in terms of reliability.

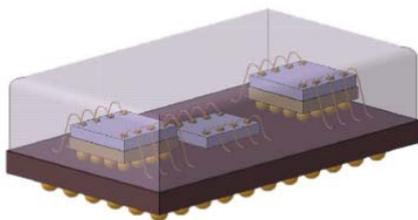
2/ 2D silicon interposers with IPD for vision care devices

The finale application of this second example is linked to the medical field, more precisely to preventive treatment for vision care. The first essential advantage IPDiA has brought forward is miniaturization of the final device in x, y and z axes. But IPDiA has also shown its ability to adapt its technology to the customer's product environment and has developed a module with four 2D silicon interposers including IPD and active components, the complete system being mounted on a 100 µm thick flexible organic substrate.



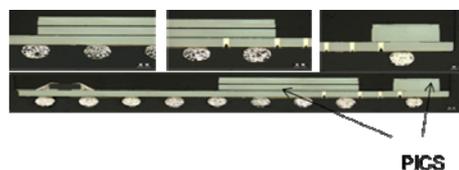
**Fig. 12:** Top view of IPDiA 2D interposer with active dies

3/ 2.5D silicon interposer with IPD for aerospace



**Fig. 13:** Motor controller device for avionic application using IPDiA 2.5D interposer technology [12]

The third example implies integrated passive devices with TSV 2.5D interposer combined with a 3D packaging technology, suitable for motor control in aerospace domain. This time, miniaturization and decrease of the total weight of the device is optimized thanks to the combination of IPD, TSV and 3D packing. Reliability is once again achieved by the silicon-silicon compatibility. IPDiA finalizes the complete module by using a stack die technology on the 2.5D interposer.



**Fig. 14:** 2.5D interposer with PICS IPD and external active dies

The work on the TSV process optimization has been led in collaboration with CEA-Leti and was part of the PRIIM project funded by OSEO.

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